

**In the abstract**

Please replace the abstract with the following revised paragraph:

129 A scheduler configured to schedule multiple channels of a [[Data]] Direct Memory Access (DMA) device includes a shift structure having entries corresponding to the multiple channels to be scheduled. Each entry in the shift structure includes multiple fields. Each entry also includes a weight that is determined based on these multiple fields. The scheduler also includes a comparison-logic circuit that is configured to then sort the entries based on their respective weights.